Application Note 512
Using the Watchdog/Alarm Counter in the DS1371 and DS1374

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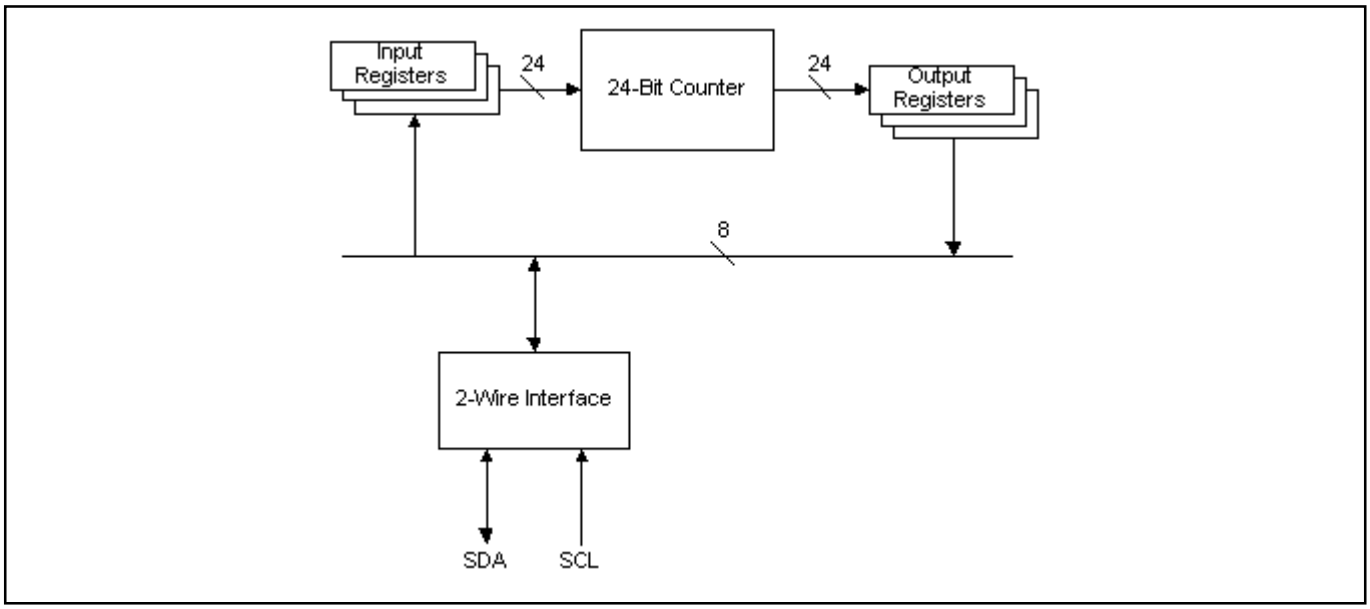
OVERVIEW

Dallas Semiconductor offers two real-time clocks that use a 32-bit counter to maintain time—the DS1371 and DS1374. Both devices also provide a 24-bit countdown watchdog/alarm counter that can provide one of three functions: a periodic alarm, a watchdog timer, or SRAM. This application note is intended to help customers understand how the counter operates and how it is configured for each function.

COUNTER CONFIGURATION

The secondary counter is mapped to the 2-wire address range 04–06h with the nomenclature WD/ALM COUNTER BYTE 0–2. These addresses are mapped to three 8-bit input registers for writes and three 8-bit output registers for reads. For a write to the device using the 2-wire interface, the input data is latched into the input register corresponding to the specified address, and the contents of all three registers are then loaded into the 24-bit counter. The input registers are used as a 24-bit seed register when the counter is reloaded. For a read from the device using the 2-wire interface, the contents of the counter are latched into the output register, and the data corresponding to the specified address is sent to the external bus. This allows the counter to decrement continuously without affecting the data being read. Figure 1 shows how these blocks interact.

Figure 1. Watchdog/Alarm Counter Configuration



CONTROL REGISTER

The control register is used to configure the watchdog/alarm counter for the DS1371 and DS1374. The registers for each device are almost identical with only bits 3 and 4 controlling device-specific functions. Both registers are detailed in the following paragraphs.

DS1371 Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{EOSC}}$	WACE	WD/$\overline{\text{ALM}}$	0	INTCN	RS2	RS1	AIE

$\overline{\text{EOSC}}$ (Enable Oscillator) – When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped. This bit is clear (logic 0) when power is first applied.

WACE (Watchdog/Alarm Counter Enable) – When set to logic 1, the WD/ALM counter is enabled. When set to logic 0, the WD/ALM counter is disabled, allowing the 24-bits to be used as SRAM. This bit is clear (logic 0) when power is first applied.

WD/$\overline{\text{ALM}}$ (Watchdog/Alarm Counter Select) – When set to logic 0, the counter provides a periodic alarm. When set to logic 1, the counter provides a watchdog timer. This bit is clear (logic 0) when power is first applied.

INTCN (Interrupt Control) – When set to logic 0, a square wave is output on the SQW/$\overline{\text{INT}}$ pin. The $\overline{\text{EOSC}}$ bit must also be enabled for the square wave to be output. When set to logic 1, the alarm flag (AF) bit in the status register asserts the SQW/$\overline{\text{INT}}$ output (provided that the alarm is also enabled). This bit is clear (logic 0) when power is first applied.

RS2 and RS1 (Rate Selects) – These bits control the frequency of the square-wave output when the square wave has been enabled. Table 1 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set (logic 1) when power is first applied.

Table 1. Square-Wave Output Frequency

RS2	RS1	FREQUENCY
0	0	1Hz
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

AIE (Alarm Interrupt Enable) – When set to logic 1, this bit permits the AF bit in the status register to assert SQW/$\overline{\text{INT}}$ (INTCN must be set). When set to logic 0 or INTCN is set to logic 0, the AF bit does not initiate the SQW/$\overline{\text{INT}}$ signal. This bit is clear (logic 0) when power is first applied.

DS1374 Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{EOSC}$	WACE	WD/$\overline{ALM}$	BBSQW	WDSTR	RS2	RS1	AIE

Only those bits that are different from the DS1371 are defined.

BBSQW (Battery-Backed Square-Wave Enable) – When set to logic 0, the SQW pin is high-impedance when V_{CC} falls below the power-fail trip point. When set to logic 1, the square-wave output remains enabled when V_{CC} is absent and the device is being powered by the V_{BACKUP} pin. This bit is clear (logic 0) when power is first applied.

WDSTR (Watchdog Reset Steering Bit) – When set to logic 0, a 250ms pulse is output on the $\overline{RST}$ pin if WD/$\overline{ALM}$ = 1 and the WD/ALM counter reaches 0. When set to logic 1, the 250ms pulse is output on the $\overline{INT}$ pin. This bit is clear (logic 0) when power is first applied.

PERIODIC ALARM

If a periodic alarm is desired, the WACE bit is set to 1 and the WD/$\overline{ALM}$ bit is set to 0. The counter then behaves as follows:

- The counter decrements every second.
- When the counter reaches 0, the AF bit in the status register is set, and the counter is reloaded with the current 24-bit value in the input registers.
- The counter is restarted.

If the AlE bit in the control register is set, the AF bit generates an interrupt on a different pin for the DS1371 and the DS1374. For the DS1371, an interrupt is generated on the SQW/$\overline{INT}$ pin if the INTCN bit is set to 1. For the DS1374, an interrupt is generated on the $\overline{INT}$ pin.

For example, the DS1371 can be configured to generate a periodic interrupt every week by enabling the counter for periodic alarms, loading the counter with the value 93A80h (7 days x 24 hours x 60 minutes x 60 seconds) and enabling the SQW/$\overline{INT}$ pin for interrupts.

WATCHDOG TIMER

If a watchdog timer is desired, the WACE bit and the WD/$\overline{ALM}$ bit are both set to 1. The counter then behaves as follows:

- The counter decrements every $^1/_{4096}$ of a second (approximately 244µs).
- If any of the WD/ALM COUNTER registers are read or written, the counter is reloaded with the current 24-bit value in the input registers and restarted.
- For the DS1371, the counter is also reloaded and restarted if there is a low-to-high transition on the WDS input.
- When the counter reaches 0, the AF bit in the status register is set, and the counter is stopped.

For the DS1371, the AF bit generates a 250ms pulse on the SQW/$\overline{INT}$ pin if the AlE and INTCN bits in the control register are set. This pulse cannot be truncated and when it is complete, the AF flag is cleared to 0 and the SQW/$\overline{INT}$ pin returns to a high-impedance state.

For the DS1374, the AF bit generates a 250ms pulse on either the $\overline{INT}$ pin or $\overline{RST}$ pin. The WDSTR bit in the control register selects on which output pin the pulse occurs. If the WDSTR is 0, the 250ms pulse occurs on the $\overline{RST}$ pin, and if WDSTR is 1, the pulse occurs on the $\overline{INT}$ pin. In either case, the pulse cannot be truncated and, when it is complete, the AF flag is cleared to 0 and the corresponding output pin returns to a high-impedance state.

For example, the DS1374 can be configured to reset a microcontroller that does not access the watchdog timer during a 150ms period. The counter is enabled as a watchdog timer, the counter is loaded with the value 266h (0.15s / 0.000244s), and steering the pulse to the $\overline{RST}$ pin.

SRAM

If neither counter type is required, the 24-bit counter can be used as 3 bytes of static RAM. This is accomplished by setting the WACE bit in the control register.

For the DS1374, which provides a backup supply input, this RAM is nonvolatile as long as the battery or super cap voltage is within specification.

SUMMARY

Because the watchdog/alarm counter provides three separate functions in one package, the DS1371 and DS1374 are cost-effective parts for a wide range of applications.